QCA XOR GATE FOR ARITHMETIC AND LOGIC CIRCUIT DESIGN

[1]NURIDDINSAFOEV, [2]JIN-SEONG LEE, [3]JUN-CHEOL JEON

[1,2,3]Department of Computer Engineering, Kumoh National Institute of Technology, Gumi, Korea
Email: [1]nuriddinsafoyev@gmail.com, [2]leejinss01@gmail.com, [*]jcjeon@kumoh.ac.kr

Abstract: The exclusive-OR(XOR) function is extensively used in microprocessors. It is a fundamental building block in many circuits, such as adders, comparators, parity checkers, multipliers, error detectors and another kind of circuits as well.In this paper, a new low-complexity single layer XOR gate is presented in QCA technology. Implementation of the gate is based on explicit interaction cell. Hence, it is not required any special equation or technique in its construction. Overall results show that the proposed gate performs better in a case of previous XOR designs. The proposed designcan be effectively realized in any more complex circuits, such as arithmetic and logic unit of QCA microprocessors.

Keywords: Nanotechnology, Quantum-Dot Cellular Automata,Exclusive-OR Gate, Quantum Computation.

I. INTRODUCTION

While exponential decreasing the feature size in CMOS (complementary metal-oxide-semiconductor) technology, devices are getting more prone to high leakage current and also getting more sensitive to circuit noise[1]. Some of the alternative nano technologies like Quantum-dot cellular automata (QCA), single electron tunneling (SET), carbon nanotube (CNT) and tunneling phase logic (TPL) can be the next stage technology in computer production. One of perspective nano-electronic technologies is the QCA based technology[2,3,5].

QCA is new device architecture and it is relevant as the nanometer scale. Computation way of this technology is based on cellular automata that composed of quantum-dot devices. The notion of QCA was introduced in 1993 by Lent et al[3].Possible physical implementations and experiments are reviewed in [4]. Micro-sized tunnel-junction QCA devices have been fabricated with metal. The device is consisted of four aluminum islands connected with aluminum oxide tunnel junctions and capacitors. It has been fabricated using electron beam lithography(EBL) and dual shadow evaporation on an oxidized silicon wafer. The switching of electrons in a cell can control in the experimentation.

However, fabrication process is not proper to mass produce QCA cellsin a small dimension for operating at room temperature. Another type of implementation is molecular QCA that has several advantages over metal dot QCA in almost all aspects, such as small cell size (10^{13} devices per cm^2), simple manufacturing process and operation at room temperature. Furthermore, switching speed is 100 times better than metal QCA.

In magnetic QCA, information is transferred via magnetic exchange interactions as opposed to the electro-static interactions in metal and molecular implementations. By the experiments, magnetic QCA using comparatively large dots(100nm in size) operates at room temperature even with current fabrication techniques. However, magnetic QCA does not appear to have the switching speed to compete with today's computers[2,6]. The clocked molecular QCA provides high device density, ultralow power dissipation and high speed switching. The design and fabrication aspects of molecular QCA are presented in [4,7,8].

QCA operates by the coulombic interaction between neighbor cells. Basically,the QCA cell is a square shape structure that consists of four quantum dots and two excess electrons. The electrons are able to move between quantum dots using tunnel junction. Depending on columbic repulsion, electrons occupy two opposite corners of the cell[9,19]. This operation creates two different polarizations such as $P = -1$ (binary 0) and $P = +1$ (binary 1) in the cell, as shown in **Fig.1**.

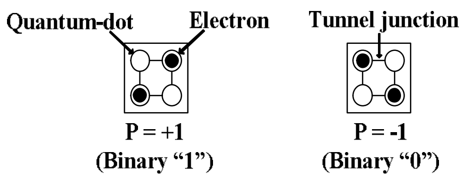


Fig.1. QCA cell with different polarizations.

Moreover, this technology has the ability to implement circuits with low latency and high speed than transistor based technology. In this paper, we propose new exclusive OR gate design with less complexity and the lowest occupation area. It does not require any wire-crossing technique.

II. RELATED WORK

2.1. QCA Preliminaries

The basic element of the QCA device is the QCA cell, as illustrated in **Fig.1**. By placing basic cells side by side, standard QCA wire is constructed, as shown in

[*] Corresponding author

Fig.2(a). This QCA wire transfers binary information due to coulombic interaction between the cells. There is also another type of QCA wire which is composed of rotated cells. It is called inverter chain and the wire is used to cross the regular QCA wire.Propagated signal is changed between two polarizations in the inverter chain[10], as illustrated in **Fig.2(b)**.

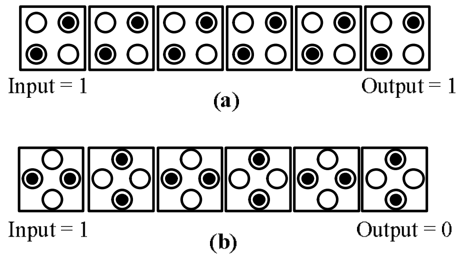


Fig.2. (a) QCA wire, (b) inverter chain

In designing QCA circuits, majority gate and QCA inverter play main role. The majority gate is composed of five QCA cells which are three input cells, one output cell and one inside cell. It is presented in **Fig.3(c)**.

$$M(A,B,0) = AB \quad \mathbf{(1)}$$
$$M(A,B,1) = A + B \quad \mathbf{(2)}$$

Basic logic gates AND gate and OR gate are implemented using the majority gate. By fixing one of the inputs to binary "0", the majority gate becomes AND gate, **eq.(1)**.Similarly, the program input is set to binary "1", the majority gate performs logic OR function[11].An inverter is constructed by placing the cells with only their corner, as demonstrated in **Fig.2(b)**.

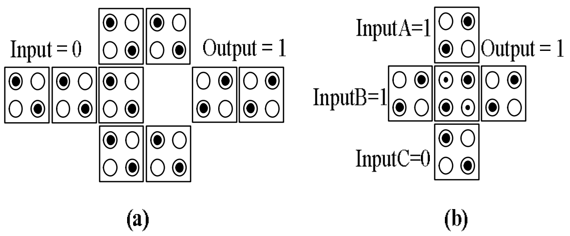


Fig.3. (a)QCA robust inverter, (b)QCA majority gate.

QCA circuit stability is based on QCA clocking which is related to adiabatic switching. A clock synchronizes signal and control information transmission as well as provides with power to run the circuit. It is realized by controlling the potential barriers between adjacent quantum dots[12]. The adiabatic switching process is described in **Fig.4(a)** and it consists of four phases: switch, hold, release and relax. Realization of adiabatic switching clock scheme in the QCA circuit requires clocking zone partition. A crucial factor of the QCA design is the clocking zone partition, because the order of appearance the four clocking zones in the circuit controls the signal flow direction in the circuit.

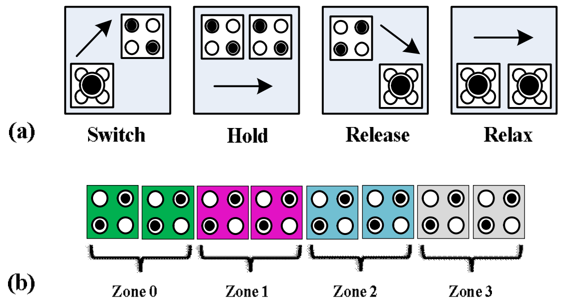


Fig.4. (a)QCA clocking, (b)clock zone.

At the beginning the switch phase, cell is unpolarized and potential barrier is down as well as barrier goes up and cells begin polarization process according to its own input cell. In the hold phase, barrier is kept high. In the third phase, barrier is getting lower. Finally, in the relax phase, cell barriers remain unpolarized[13,14].

2.2. QCA based XOR gates

In digital circuits, exclusive-OR gate is extensively used in arithmetic applications. It is the main part of such circuits: adders, error detection and correction applications.Functionality of this circuit is presented in **eq.3**.

$$XOR(A \oplus B) = \bar{A}B + A\bar{B} \quad \mathbf{(3)}$$

We have reviewed some prior works that were proposed better QCA XOR designs [15,16]. In the paper [15], authors proposed XOR gate using five input majority gate, as illustrated in **Fig.5**. This design is required 67 cells and desired output is generated after five clock phases. Single layer wire-crossing is implemented in this layout.

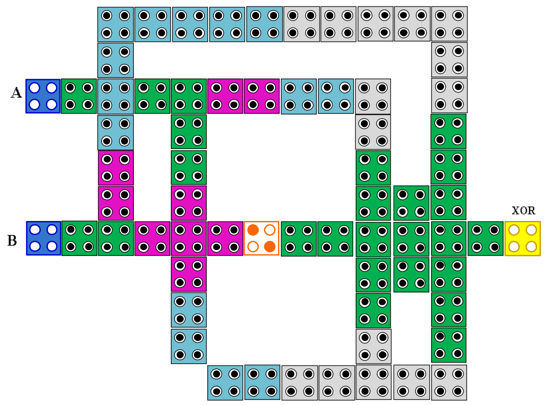


Fig.5. Design of XOR gate by Angizi et al.

There arethree kinds of wire crossing such as coplanar crossing, multilayer-wire crossing and single layer wire crossing in QCA technology[12]. The previous design uses single layer wire-crossing technique that is realized based on QCA clocking. Coplanar wire crossing is constructed by rotated cells as inverter chain. Moreover, multilayer-wire crossing technique is also used widely.

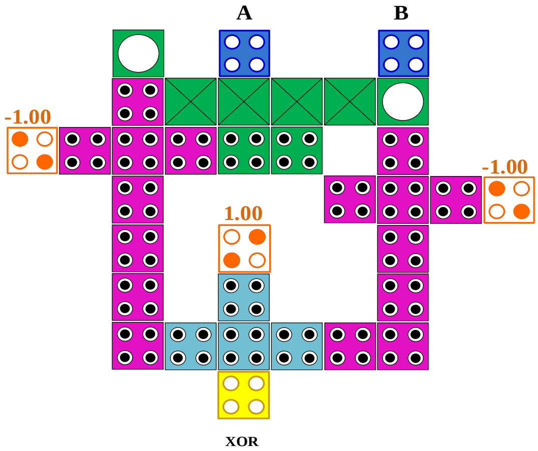


Fig.6. Design of XOR gate by Mohammadi et al.

In **Fig.6**, multilayer based XOR gate structure is presented by Mohammadi et al[16]. This design employs 39 cells and its delay is equal to three clock phases. When we check this layout in QCADesigner tool[17], the simulation result indicates that the strength of the signal is not good enough.

III. PROPOSED STRUCTURE

3.1. New XOR design in QCA

In this paper, we propose a new XOR gate design in QCA, as illustrated in Fig.7. Several QCA XOR gates are presented by researchers [15,16,18]. Most of them require majority gates and inverters for their construction process. Furthermore, their clocking and occupation area aspects are also high. Our proposed design does not require any wire-crossing technique and it has only 14 cells with two clocking phases.

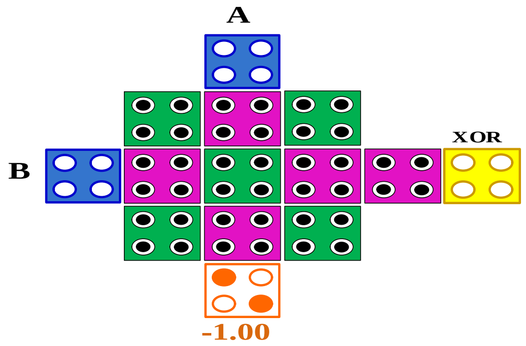


Fig.7. Proposed XOR design in QCA.

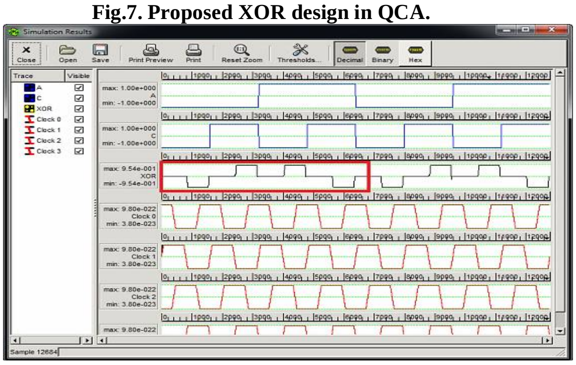


Fig.8. Simulation result of the proposed XOR gate.

3.2. Comparison and Analysis

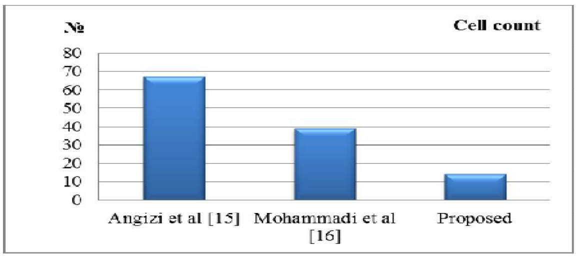
We use to design and simulate the proposed design with QCADesigner tool version 2.0.3 that is an accurate simulation tool for QCA circuits. The simulation result of the proposed design is demonstrated in **Fig.8**. The result confirms that the expected output of the proposed design is achieved correctly. The XOR gate is built using 14 cells on approximately $0.01\ \mu m^2$ area.

Table.1 shows the result of performance and analysis of the proposed design with previous QCA XOR designs in terms of the cell count, latency, occupied area and wire-crossing aspects.

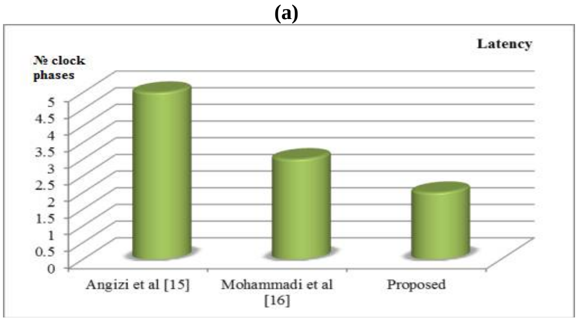
	Cell count	Latency	Area (μm^2)	Wire-crossing
Angizi et al[15]	67	5	0.05	Single layer
Mohammadi et al [16]	39	3	0.03	Multi-layer
Proposed	14	2	0.01	No wire crossing

Table.1. Comparison of QCA XOR gates

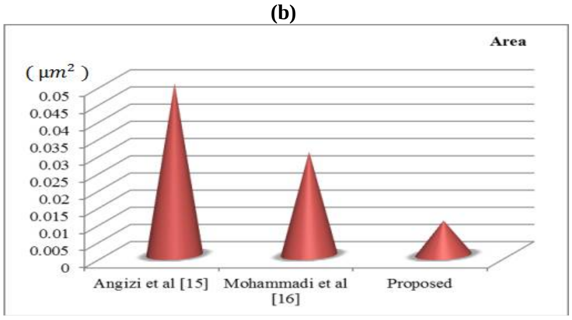
The number of used cells in a QCA circuit is generally proportional to its area. Hence, decreasing number of used cell is relatively improvement to the circuit area. The area is also dependent on wire-crossing types. An important metric in assessing the performance of circuits is delay, namely QCA clocking.



(a)



(b)



(c)

Fig.9. (a)Cell count comparison, (b)Latency comparison, (c)Total area comparison diagrams among QCA XOR's.

The main QCA circuit metrics such as cell count, area and latency aspects have been analyzed among the QCA XOR designs according to **Table.1** and the table results are represented as diagramin **Fig.9**. As claimed by the diagrams, it can be observed that our design has achieved in terms of cell count 79% and 64%, its occupation area 80% and 67% improvements in comparison with [15] and [16] designs, respectively. In addition, the latency of our design is also improved relatively.

CONCLUSIONS

This paper has presented an efficient and novel design of XOR gate in QCA. By utilizing this gate to combinational and sequential circuits, we can achieve significant improvements in terms of circuit complexity, such as latency and area aspects. The proposed design is better than the existing QCA XOR circuits in comparison. The presented layout can be easily used to design in complex circuits.Designing arithmetic and logic unit (ALU) architecture in QCA is our future work. There exist further opportunitiesfor optimization which could lead to densities greaterthan reported in this work and could be takenup for further studies.

ACKNOWLEDGMENTS

This work was supported by the National Research Foundation of Korea(NRF) grant funded by the Korea government(MSIP) (NO. NRF-2015R1A2A1A15055749).

REFERENCES

1. R. Compano, L.Molenkamp and D.J. Paul, “Technology Roadmap for nanoelectronics 2000”, European commission IST Programme-Future and Emerging Technologies, 2001.
2. A.O. Orlov, I. Amlani, G.H. Bernstein, C.S. Lent and G.L. Snider, “Realization of a functional cell for quantum-dot cellular automata”, Science 277,pp.928–930,1997.
3. C.S. Lent, P.D. Tougaw, W. Porod and G.H. Bernstein, “Quantum cellular automata”, Nanotechnology 4, pp.49–57, 1993.
4. G.H. Bernstein, “Quantum-dot cellular automata: computing by field polarization”, Proceeding of Design Automation Conference, pp.268–273, 2003.
5. T.N. Sasamal, A.K. Singh and A. Mohan, “An optimal design of full adder based on 5-input majority gate in coplanar quantum-dot cellular automata,” International Journal for Light and Electron Optics, vol.127, pp.8576–8591, 2016.
6. R. Farazkish and F. Khodaparast, “Design and characterization of a new fault-tolerant full-adder for quantum-dot cellular automata”, Microprocessors and Microsystems Journal, vol.39, pp.426–433, 2015.
7. M.T. Niemier, R. Ravichandran and P.M. Kogge, “Using circuits and system-level research to drive nanotechnology,” IEEE Conference on Computer design, pp.302–309, 2004.
8. M. Gladshtein, “Quantum-dot cellular automata serial decimal processing-in-wire: Run-time reconfigurable wiring approach,” Microelectronics Journal, vol.55, pp.152–161, 2016.
9. J.C. Jeon, “Extendable Quantum-Dot Cellular Automata Decoding Architecture Using 5-Input Majority Gate,” International Journal of Control and Automation, vol.8, no.12, pp.107–118, 2015.
10. J.C. Jeon, “Low Hardware Complexity QCA Decoding Architecture Using Inverter Chain,” International Journal of Control and Automation, vol.9, no.4, pp.347–358, 2016.
11. M.B. Tahoori, J. Huang, M. Momenzadeh and F. Lombardi, “Testing of quantum cellular automata,” IEEE Trans. On Nanotechnology, vol.3, no.4, pp.432–442, 2004.
12. K. Makanda and J.C. Jeon, “Combinational circuit design based on Quantum-dot Cellular Automata,”International Journal of Control and Automation,vol.7, pp.52–57, 2014.
13. Y. Wang and M. Lieberman, “Thermodynamic behavior of molecular-scale quantum-dot cellular automata (QCA) wires and logic devices,” IEEE Trans. On Nanotechnology, vol.3, pp.368–376, 2004.
14. N. Safoev and J.C. Jeon, “Low area complexity demultiplexer based on multilayer Quantum-dot Cellular Automata,” International Journal of Control and Automation, vol.9, pp.165–178, 2016.
15. S. Angizi, E. Alkaldy, N. Bagherzadeh and K. Navi, “Novel Robust Single Layer Wire Crossing Approach for Exclusive OR Sum of Products Logic Design with Quantum-Dot Cellular Automata,” Journal of Low Power Electronics, vol.10, pp.256–271, 2014.
16. M. Mohammadi, S. Gorgin and M. Mohammadi, “Design of non-restoring divider in quantum-dot cellular automata technology,” IET Journals, vol.11, pp.135–141, 2017.
17. K. Walus, T.J. Dysart, G.A. Jullien and R.A. Budiman, “QCADesigner: A rapid design and Simulation tool for quantum-dot cellular automata,” IEEE Transactions on Nanotechnology, vol.3, pp.26–31, 2004.
18. W. Sen and C. Li, “Novel Exclusive-OR Gate and Full Adders Implementation using Quantum Cellular Automata”, Trans Tech Publications, vol.121, pp. 565-570, 2007.
19. J. S. Lee and J. C. Jeon, "Design of Low Hardware Complexity Multiplexer Using NAND Gates on Quantum-Dot Cellular Automata," International Journal Multimedia and Ubiquitous Engineering, Vol.11, No.12, pp.307-318, 2016.

★★★