DESIGN OF A LOW POWER CMOS IMAGE SENSOR WITH A HYBRID CORRELATED DOUBLE SAMPLING FOR MOBILE SENSOR NETWORKS

[1]MINHYUN JIN, [2]JOONGHO CHOI, [3]MINKYU SONG

[1,3]Department of Semiconductor Science, Dongguk University, Seoul, Korea
[2]Department of Electrical and Computer Engineering, University of Seoul, Korea
E-mail: [3]mksong@dongguk.edu , [2]jchoi@uos.ac.kr

Abstract - A low power CMOS Image Sensor(CIS) has a great role to implement mobile sensor networks. In this paper, a low power CIS with a hybrid Correlated Double Sampling (CDS) scheme is discussed. In order to improve the CIS performance, a mixed mode scheme composed of both an analog CDS and a digital CDS is proposed. With the technique, we can drastically reduce both the column Fixed Pattern Noise (FPN) and the power consumption. The prototype sensor was fabricated with a TowerJazz 0.18μm CIS technology and the pixel pitch is 2.2μm. The measured column FPN is 0.10 LSB and the power consumption is only 10mW at the 2.8V power supply voltage with 176x144 pixels

Keywords - Low power CMOS Image Sensor, mobile sensor network, hybrid correlated doubling sampling, column fixed pattern noise

I. INTRODUCTION

CMOS image sensors have been widely used in various applications such as digital cameras, digital camcorders, CCTV, car security cameras, medical equipment, and so on. In order to improve the image quality, many kinds of studies to have a low level of noise have become a major concern. In particular, fixed pattern noise (FPN) generated by non-uniformity of pixels and readout circuits including analog to digital converters (ADC) is a major factor of noise in a column-parallel CMOS image sensor [1]-[5]. In general, an analog correlated double sampling (CDS) circuit, which consists of capacitors and switches, has been widely used to eliminate the FPN. Although the analog CDS circuit is easy to design and operate, it is difficult to improve the accuracy when using this circuit because of a capacitance mismatch, a clock feed-through error at the switch, and so on. On the contrary, a digital CDS [1][2] or dual CDS [3]-[5] that uses both analog CDS and digital CDS enables the resolution of CDS to improve beyond 10-bit. Nevertheless, they also have a few drawbacks. Fundamentally, they have a low conversion speed because of digital double sampling for comparison of the reset and the signal. Furthermore, the double memory type of dual CDS consumes a bigger area and more power consumption because the architecture needs an 11-bit global counter and two 11-bit memories in every column to achieve 10-bit resolution. Although high speed CMOS image sensors based on a column counter have been recently reported in [2]-[5], they use a complex design and their power consumption and chip area are still large for the applications that require low power and a small pixel pitch. In this paper, a CMOS image sensor with a column-parallel single-slope ADC (SS-ADC) and a mixed-mode dual CDS which consists of an analog CDS circuit and a digital CDS circuit is described. To realize a low power consumption and a low digital switching-noise without decreasing the speed, a new and simple digital CDS which has a satisfactory resolution of 10-bit or beyond is presented. This paper is organized as follows. Section II describes the architecture of the proposed CMOS image sensor. Section III shows the circuit description of the image sensor. Section IV presents the measurement results. Finally, the conclusion and directions for future work are provided in Section V.

II. ARCHITECTURE

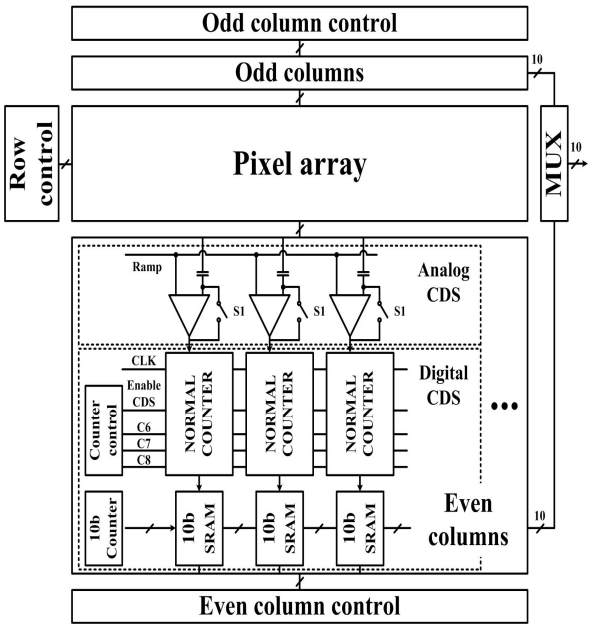

Fig.1 Block diagram of the proposed CMOS image sensor.

Fig. 1 shows the block diagram of the proposed CMOS image sensor. The image sensor is composed of a pixel array, two side column parallel readout circuits, and digital control blocks. The column parallel readout

circuit is based on a single-slope analog-to-digital converter (SS-ADC). Further, it is composed of both an analog CDS and a digital CDS to improve the noise characteristics and conversion speed. The digital CDS consists of a normal counter and a SRAM.

The pixel array is based on a 4-transsitor two-shared pinned-photodiode with a pixel pitch of 2.2μm. A row control block, a column control block, and a multiplexer (MUX) are included in the digital control block. The two side column structure – with odd columns and even columns – expands the column pitch from 2.2μm to 4.4μm, thereby preventing errors generated by small column pitch.

III. CIRCUIT DESCRIPTION

A. An Analog CDS with a Single-Slope ADC

Fig.2 shows the circuit diagram of the pixel and analog CDS. The pixel is composed of four transistors except V_{BIAS} transistor and one photodiode. Then, the output of pixel V_{PIX} is transferred into the analog CDS block. Normally the analog CDS block is composed of a single-slope analog-to-digital converter with a comparator, a ramp signal generator, and a digital counter. A novel comparator shown in Fig.2 is proposed in this paper. It is composed of a cascode bias technique and a nMOS cross coupled latch style to increase the comparator gain. With the comparator circuit, the voltage gain of the comparator is much higher than that of the inverter style comparator [2].

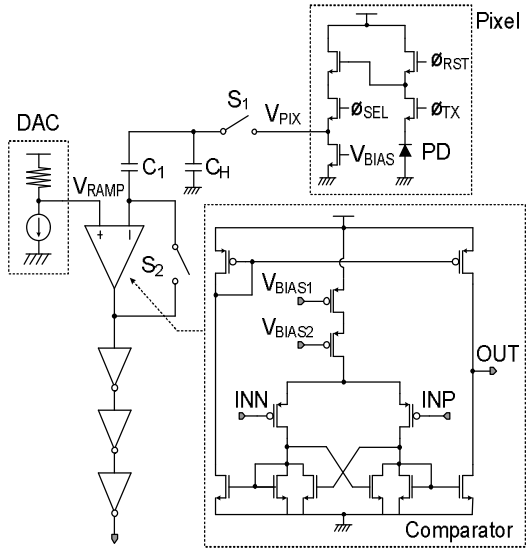

Fig.2 Circuit Diagram of Pixel and Analog CDS

Fig.3 shows the principle and the circuit diagram of a single-slope ADC. With the switches and the capacitors, the analog signal $V_{IN}=V_{RST}-V_{SIG}$ is transferred to the input of comparator. Then, the ramp generator starts its voltage increasing. Simultaneously, the normal counter also starts its counting. When the voltage of ramp generator is equal to the voltage of V_{IN} , the digital code of comparator is changed into zero. After the digital code of comparator is changed, the counter stops its counting. Then, the digital codes of counter are stored into SRAM. This is a normal processing of the single-slope ADC. It is very simple and easy to implement. However, the most difficult problem is that all of them are integrated into a very small pitch like 2.2um or 4.4um.

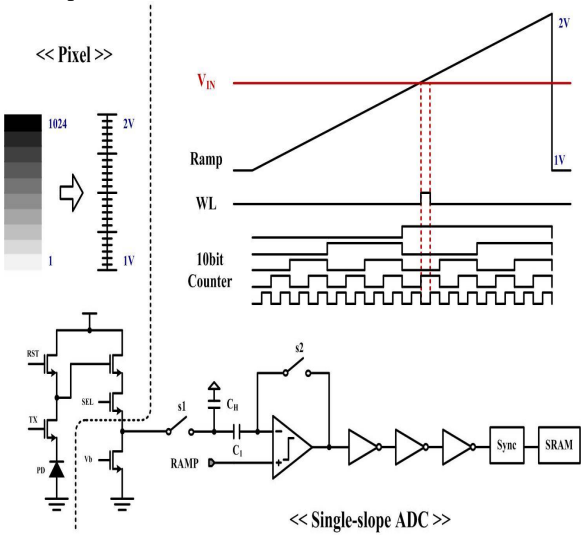

Fig.3 Processing of the single-slope ADC

B. Mixed-mode Dual CDS

A mixed-mode dual CDS architecture composed of both an analog CDS and a digital CDS has an advantage of reducing noise and improving conversion speed. Further, the power consumption of dual CDS architecture is normally lower than that of the digital CDS. The main advantage of the dual CDS is that it has a high noise suppression capability because the fixed pattern noise (FPN) cancellation is performed in both the analog domain and the digital domain. Additionally, in this paper, the analog CDS, which reduces the ADC period for the reset voltage by eliminating the analog offset of the pixel and the comparator output, enables high speed conversion and low power consumption because a normal counter in each column is sufficient to provide the desired 10-bit resolution.

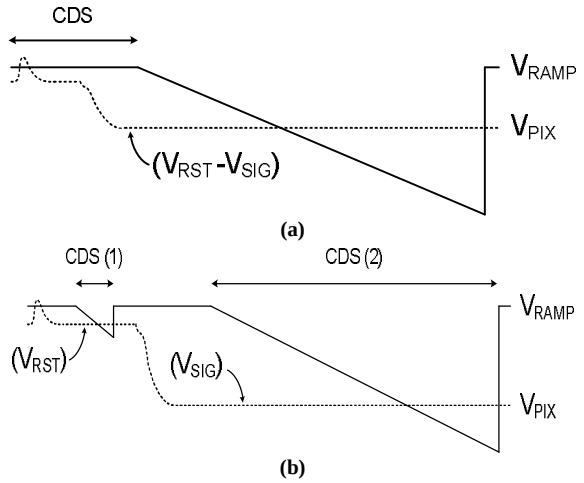

Fig.4 Principles of Correlated Double Sampling. (a) Analog CDS (b) Digital CDS

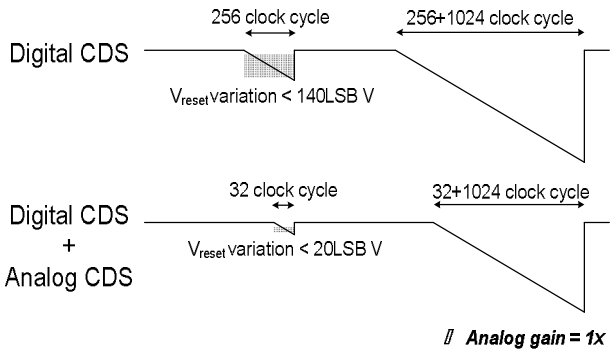

Fig.5 The Advantage of the Mixed-mode Dual CDS.

Fig.4 shows the principles of both the analog CDS and digital CDS. In case of analog CDS shown in Fig.4 (a), since the value of V_{RST}-V_{SIG} is obtained at the input of comparator, the desired digital codes are directly transferred into SRAM. On the contrary, in case of digital CDS shown in Fig.4(b), the analog value of V_{RST} and V_{SIG} are directly converted into digital codes, respectively. Then, we get the final digital code of V_{RST}-V_{SIG} with a digital subtractor. Therefore, each CDS has its own advantages and drawbacks. Although the period of A/D conversion for the reset voltage is reduced by using analog CDS in the dual CDS architecture, the required bit number of counter is increased when the slope of the ramp signal is decreased for high analog gain. The high analog gain changes the total level of light into bright level and makes it easy to distinguish the light level, despite reducing treatable range of light input. Fig. 5 shows the advantage of the mixed-mode CDS

IV. MEASRUREMENT RESULTS

The prototype CMOS image sensor was fabricated by a 0.18μm TowerJazz CIS process. A pixel array of 176×144 was implemented with 2.2μm pixel pitch. The column pitch is 4.4μm by using a two side column structure. Although the effective chip area is 1.8mm×1.7mm, the total chip area including bonding pads is 2.35mm×2.35mm. Fig. 6 shows the chip microphotograph. We employ an off-chip field programmable gate array (FPGA) to generate the various clock signals controlling the image sensor, and change the signals flexibly. Fig.7 shows the photos of the measurement systems. To generate the clock signals, we transfer the Verilog code from the computer to the FPGA through a USB interface. After that, the FPGA transfers the clock signals to the image sensor, receives data outputs from the image sensor, and transfers the outputs to the computer, simultaneously. The sensor board is composed of variable resistors, regulators, and the image sensor chip with a lens. The FPGA and a DAC generating the ramp signal are included in the main-board. Fig. 8 shows the measured results of sample images. Therefore, the proposed mixed-mode dual CDS has the excellent performance with very low power consumption.

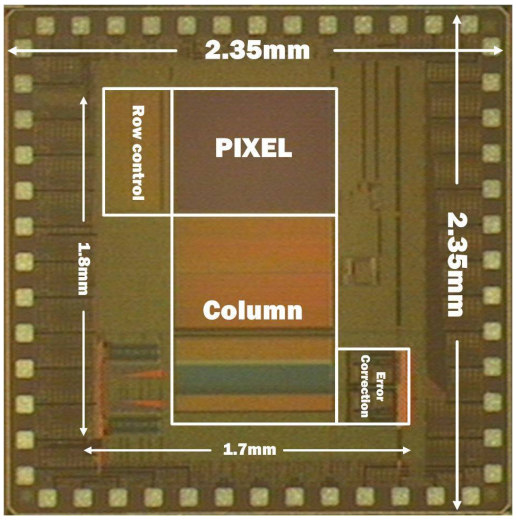

Fig. 6 Chip Microphotograph.

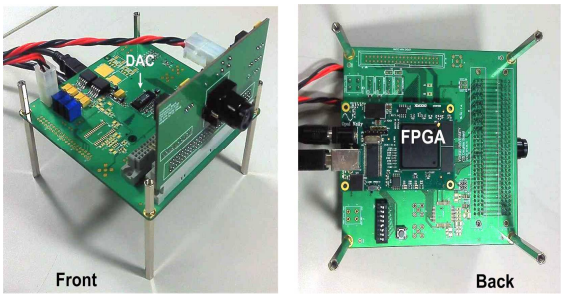

Fig. 7 Photograph for the CIS Measurement Systems

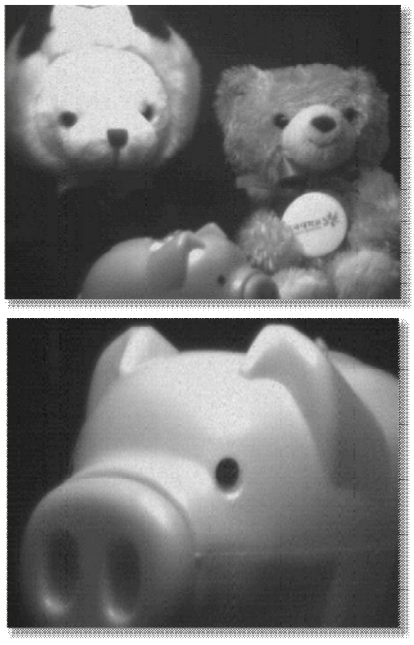

Fig. 8 Measured Sample Images

CONCLUSIONS

This paper has presented a CMOS image sensor with a mixed-mode dual CDS for a 10-bit 176×144 pixel, 80 frame/s specifications. As well as an analog CDS with a novel comparator has been proposed, a mixed-mode dual CDS reduced the power consumption drastically. In conclusion, there were three main advantages of a

mixed-mode dual CDS technique. First, the proposed CMOS image sensor and conventional one were based on the column-parallel SS-ADC with almost the same architecture. Thus, a low noise image sensor was implemented by minimally changing the design of a conventional image sensor. Secondly, the proposed algorithm made it possible to increase the frame rate with relatively low power and small area, and the digital CDS enhanced energy efficiency. Thirdly, it was possible to adapt the techniques to other digital CDSs, even in high speed digital CDSs. The chip performance is summarized in Table I. The measured column FPN is about 0.1LSB with the proposed dual CDS.

Process	0.18μm TowerJazz CIS
Chip size	2.35mm×2.35mm
Effective chip size	1.7mm×1.8mm
Resolution	176×144 (QCIF)
Pixel size	2.2μm×2.2μm
Supply voltage	2.8V (analog), 1.5V (digital)
Frame rate	80 frame/s
ADC resolution	10-bit
Column FPN	0.10LSB (with mixed mode CDS)
Power consumption	10mW

Table1: Measured Results

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